Low Frequency Noise in MoS_2 Negative Capacitance Field-effect Transistor

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***Abstract*—In this work, we report on low frequency noise studies in MoS_2 NC-FETs for the first time. Low frequency noise of the devices is systematically studied depending on various interfacial oxides, different thicknesses of interfacial oxide, and ferroelectric $H_{0.5}Z_{0.5}O$ (HZO). The low frequency noise is found to decrease with thicker ferroelectric HZO in the subthreshold regime of the MoS_2 NC-FETs, in stark contrast to the conventional high-*k* transistors. This result can be interpreted as electrostatic improvement induced by the negative capacitance effect. It demonstrates that negative capacitance can not only improve the device performance in the on- and off-states, but also suppress the noise of the devices.**

***Index Terms*—hafnium zirconium oxide, low frequency noise, molybdenum disulfide, negative capacitance field-effect transistors.**

I. Introduction

The integration of negative capacitance using ferroelectric insulator in gate stack has triggered intensive research interest recently as one of the emerging solutions to achieve subthreshold swing (SS) below the Boltzmann limit of 60 mV/dec at room temperature for a metal-oxide-semiconductor field-effect transistor (MOSFET) [1-11]. Meanwhile, 2-dimensional (2D) semiconductors, such as transition metal dichalcogenides (TMDs), have the potential for ultra-scaled transistor technology beyond the 10 nm technology node because of their atomically thin layered structures and low dielectric constant, which offers strong electrostatic control [10, 11]. Recently, MoS_2 negative capacitance field-effect transistors (NC-FETs) have been demonstrated with sub-thermionic SS and non-hysteretic transfer characteristics, suggesting the potential for 2D NC-FETs for future ultra-scaled and low power digital applications [2, 9, 10]. The 2D semiconductor and its interface to ferroelectric gate stack in MoS_2 NC-FETs may present unique interface and ferroelectric properties. Low frequency noise characterizations can be utilized to quantitatively analyze the performance and reliability of these devices [14-17]. However, there have not yet been any studies on the low frequency noise on 2D NC-FETs.

Herein, we report on low frequency noise studies on MoS_2 NC-FETs with relatively large channel areas (3~11 μm^2). Low frequency noise is systematically studied for various interfacial oxides, and with different thicknesses of interfacial oxide on top of the ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ (HZO). The low frequency noise is found to decrease with thicker ferroelectric HZO in the subthreshold regime of a MoS_2 NC-FET, because thicker HZO leads to stronger negative capacitance effect and thus larger series of gate capacitance and better electrostatic control of the channel. The existence of negative capacitance in ferroelectric HZO facilitates a new approach to suppress the noise of the semiconductor devices.

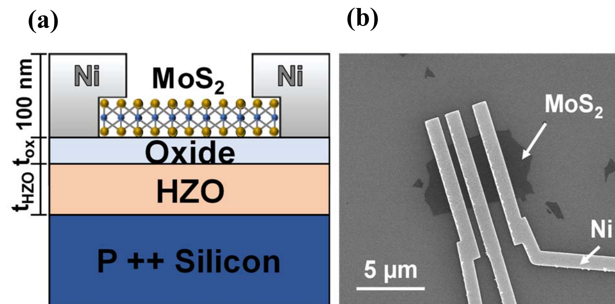

Fig. 1. (a) Schematic diagram of a MoS_2 NC-FET. The device includes the p++ Si as gate electrode, HZO as the ferroelectric layer, Al_2O_3, HfO_2, or ZrO_2 as the oxide layer and 100 nm Ni as source/drain contacts. (b) Top-view SEM image of two MoS_2 NC-FETs, capturing the MoS_2 flake and Ni electrodes.

II. Experiments

Fig. 1 (a) shows a schematic view of a MoS_2 NC-FET. The NC-FET devices presented in this study consist of a few-layer MoS_2 flake as the channel, and a gate stack composed of an amorphous interfacial oxide (Al_2O_3, ZrO_2, or HfO_2) and polycrystalline HZO employed as a ferroelectric oxide on a heavily doped silicon substrate as the gate electrode and nickel source/drain (S/D) contacts. Fig. 1 (b) shows a top-view of a Scanning Electron Microscopy (SEM) image of two MoS_2 NC-FETs fabricated on the same MoS_2 flake with different channel lengths. Table I summarizes the different gate stacks of the samples studied in this work. MoS_2 NC-FETs were fabricated as follows: HZO film was deposited by atomic layer deposition (ALD) at 250 ºC on a heavily p-doped (p++) silicon substrate that was cleaned by standard solvent cleaning, BOE dip, and deionized water rinse. TDMAHf, TDMAZr, and H_2O were used as Hf precursor, Zr precursor, and oxygen precursor, respectively. Another Al_2O_3, ZrO_2, or HfO_2 layer was subsequently *in-situ* deposited by ALD at the same temperature. Then, rapid thermal annealing (RTA) in nitrogen

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ambient for 1 minute at 500 °C was performed. MoS_2 flakes were transferred afterward to the substrate by mechanical exfoliation. Fig. 2 shows the Atomic Force Microscopy (AFM) measurement of a typical exfoliated flake with thickness controlled between 4 nm and 10 nm. Electrodes of 100 nm nickel were fabricated by an electron-beam lithography, electron-beam evaporation, and lift-off process. All electrical and noise measurements were performed in air at room temperature using a Keysight B1500/B1530A system.

TABLE I. DESCRIPTION OF THE SAMPLES AND DEVICE DIMENSIONS.

SAMPLE	1	2	3	4	5	6	7
MoS_2 (4~10 nm)							
Al_2O_3 (nm)	-	-	0.5	1	2	2	2
HfO_2 (nm)	1	-	-	-	-	-	-
ZrO_2 (nm)	-	1	-	-	-	-	-
HZO (nm)	20	20	20	20	20	15	35

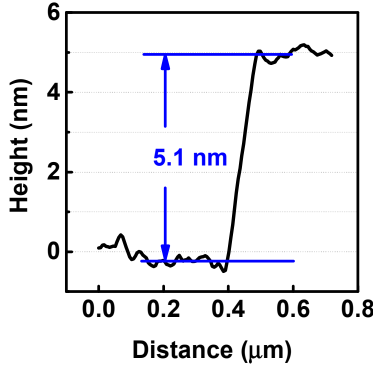

Fig. 2. Typical MoS_2 flake thickness measured by AFM for a MoS_2 NC-FET.

III. RESULTS AND DISCUSSION

The polarization vs. voltage (P-V) is directly measured on a ferroelectric capacitor with a 100 nm Ni/3 nm Al_2O_3/20 nm HZO/n++ Si structure at different frequencies using Radiant Precision LC II test system at a 10 V voltage sweep range. The polarization charge is internally measured by applying the stimulus signal on the capacitor and integrating the measured current passing through the capacitor to compute the charge. Clean hysteresis loops can be observed as shown in Fig. 3(a). The P-V characteristics as a function of the voltage sweep range at 100 Hz are shown in Fig. 3(b). Both remnant polarizations and coercive field increase with larger voltage sweep range, indicating the polycrystalline nature of the ferroelectric HZO. Different grains can provide different remnant polarizations and coercive fields due to the different domain sizes and crystal orientations.

I_D-V_{DS} characteristics of a MoS_2 NC-FET with 2 nm Al_2O_3/20 nm HZO at room temperature, low V_{GS}, and low V_{DS} conditions are plotted in Fig. 4, where I_D is the drain current and

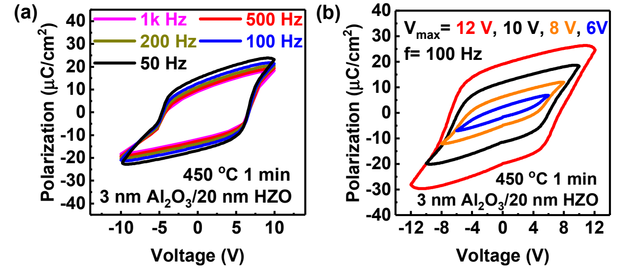

Fig. 3. (a) Hysteresis loops of P-V for 20 nm HZO/3 nm Al_2O_3 annealed at 450 ºC, measured from 50 Hz to 1 kHz. (b) Hysteresis loops of P-V for 20 nm HZO/3 nm Al_2O_3 annealed at 450 ºC at voltage sweep ranges from 6V to 12 V.

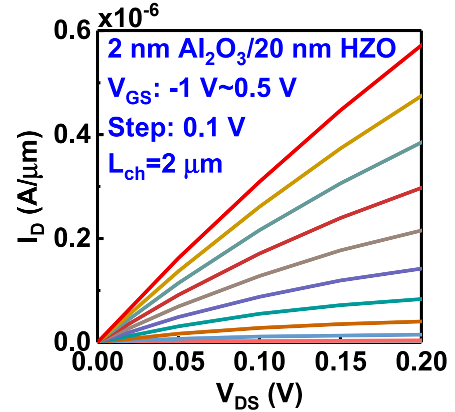

Fig. 4. I_D-V_{DS} characteristics of a MoS_2 NC-FET measured at room temperature, W_{ch}=5.7 μm. The transistor exhibits good switching behavior ($I_{on}/I_{off}>10^6$), with linear relationship between I_D and V_{DS} which also confirms minimal effect of the S/D Schottky barriers.

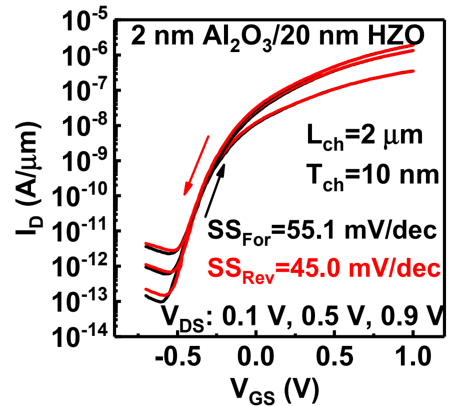

Fig. 5. I_D-V_{GS} characteristics of a MoS_2 NC-FET measured at room temperature. This device has a L_{ch} of 1 μm, W_{ch} of 5.7 μm, channel thickness of 10 nm, and 2 nm Al_2O_3 and 20 nm HZO as gate dielectric.

V_{DS} is the drain-source voltage. This device has a channel length (L_{ch}) of 2 μm and channel thickness (T_{ch}) of 10 nm. Fig. 5 shows the I_D-V_{GS} characteristics of the same device at room temperature, measured at V_{DS} voltages of 0.1 V, 0.5 V, and 0.9 V. The I_D-V_{GS} characteristics are measured using bi-directional sweeps (sweeping the gate voltage from low to high then from high to low voltages, with sweep time of 1 minute for each V_{DS} bias). No significant hysteresis can be observed on this device (less than 5 mV measured at 0.1 nA/μm). The device also displays good switching behavior ($I_{on}/I_{off} > 10^6$), and a linear

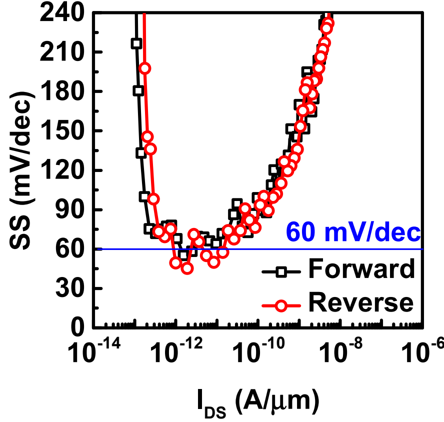

Fig. 6. SS vs. I_D characteristics of the same device as in Fig. 5. SS less than 60 mV/dec is obtained for both forward and reverse gate voltage sweep directions.

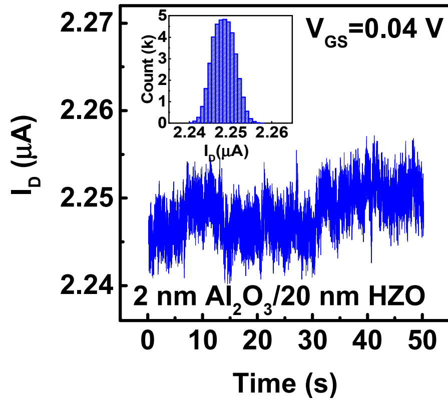

Fig. 7. A typical I_D fluctuation vs. time measured at V_{GS}=0.04 V for a MoS_2 NC-FET with 2 nm Al_2O_3/20 nm HZO as gate dielectric.

relationship between I_D and V_{DS}, which indicates a minimal effect on measured I_D noise from S/D Schottky barriers. Fig. 6 shows SS vs. I_D at the off-state of the device. The MoS_2 NC-FET exhibits SS for forward sweep and for reverse sweep of 55.1 mV/dec and 45.0 mV/dec, respectively, which are below the 60 mV/dec limit in both sweeps.

To examine drain current fluctuation, I_D vs. time characteristics are measured at constant V_{GS} and V_{DS} biases after a few seconds hold time (V_{DS} throughout this work chosen to be 0.1 V unless otherwise specified, in which to ensure that the device is operated in linear mode). Fig. 7 shows measured I_D vs. time during low frequency noise measurement. No obvious I_D (or V_T) drifting can be observed, suggesting bias temperature instability (BTI) is not a concern during this measurement (less than 100 seconds of a stress) and all charge trapping is screened during the initial hold time.

The power spectral density of drain current fluctuation (S_{ID}) is calculated based on the measured I_D vs. time characteristic. Fig. 8 shows the normalized power spectral density (S_{ID}/I_D^2) vs. frequency of a MoS_2 NC-FET with L_{ch}= 2 μm, 5.7 μm channel width (W_{ch}), and 2 nm Al_2O_3/20 nm HZO as gate dielectric, measured for different gate voltages. Each sweep shows a clear 1/*f* characteristic. S_{ID}/I_D^2 as a function of

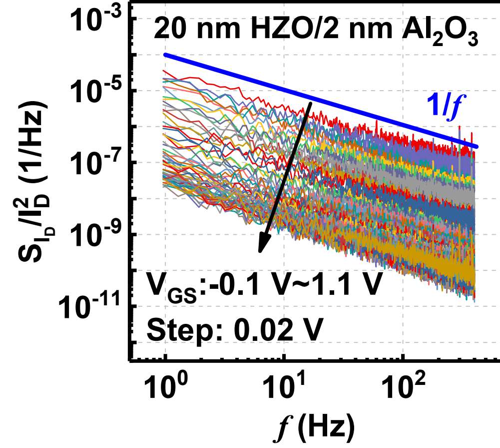

Fig. 8. Normalized power spectral density for a certain range of applied gate voltages V_{GS} on a MoS_2 NC-FET with 2 nm Al_2O_3/20 nm HZO as gate dielectric.

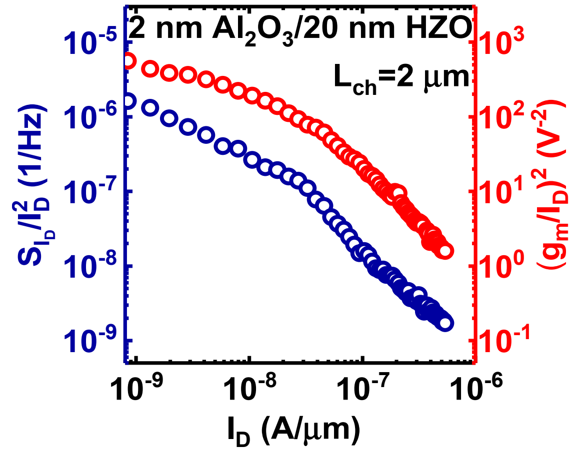

Fig. 9. Normalized I_D noise at f=10 Hz for a MoS_2 NC-FET with 2 nm Al_2O_3/20 nm HZO as gate dielectric. The non-linear behavior at low drain current and the proportional scaling with $(g_m/I_d)^2$ indicates charge number fluctuation to be the source of the low frequency noise measured in this work.

I_D at single frequency f=10 Hz of the same device is depicted in Fig. 9. In this figure, S_{ID}/I_D^2 vs. I_D deviates from a linear curve and is proportional to $(g_m/I_D)^2$. This suggests carrier number fluctuation (CNF) contributing to the low frequency noise rather than carrier mobility fluctuation. S_{ID}/I_D^2 as a function of V_{DS} at f=10 Hz is shown in Fig. 10 for MoS_2 NC-FETs with 2 nm Al_2O_3 and HZO thickness varying from 15 nm to 35 nm as the gate dielectrics. Here, although the noise from the Schottky contacts reduces with increased V_{DS}, the dependence of power spectral density above V_{DS}=0.1 V is weak, which also confirms that the noise measured comes from the channel instead of Schottky contact resistance [14]. Therefore, CNF inside the MoS_2 channel is verified as the main noise source for MoS_2 NC-FETs in this work. From the well established model for carrier number fluctuation, the drain current noise varies approximately as in eqn. (1) for the above threshold region and eqn. (2) for the subthreshold region [13],

$$\frac{W_{ch}L_{ch}S_{I_D}}{I_D^2} = \frac{q^2kT\lambda N_t}{f^{\gamma}C_{EOT}^2(V_{GS}-V_T)^2} \propto \frac{q^2g_m^2\,kT\lambda N_t}{f^{\gamma}} \quad (1)$$

$$\frac{W_{ch}L_{ch}S_{I_D}}{I_D^2} = \frac{q^4\lambda N_t}{kTf^{\gamma}(C_{ox}+C_d+C_{it})^2} \quad (2)$$

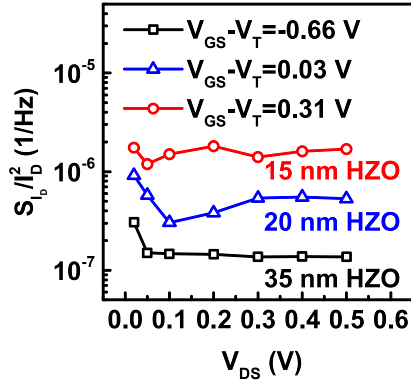

Fig. 10. Normalized I_D noise vs. V_{DS} at f=10 Hz for MoS_2 NC-FETs with 2 nm Al_2O_3 and HZO from 15 nm to 35 nm as gate dielectric.

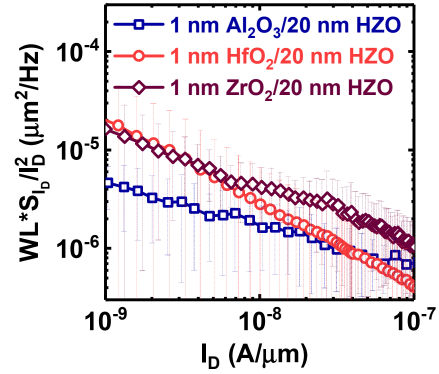

Fig. 11. Normalized I_D noise vs. I_D at f=10 Hz for MoS_2 NC-FETs with 1 nm different interfacial oxide and 20 nm HZO as gate dielectric.

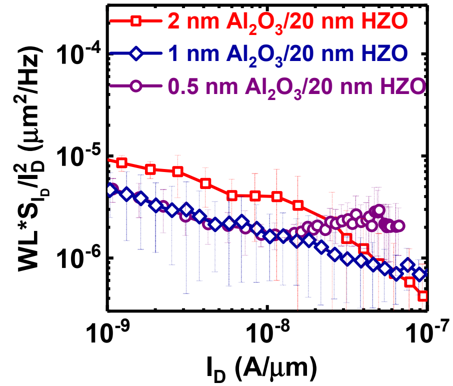

Fig. 12. Normalized I_D noise vs. I_D at f=10 Hz for MoS_2 NC-FETs with 0.5/1/2 nm Al_2O_3 and 20 nm HZO as gate dielectric.

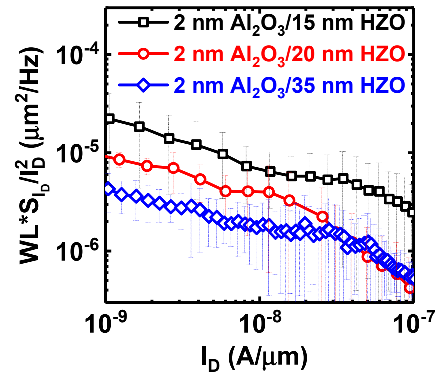

Fig. 13. Normalized I_D noise vs. I_D at f=10 Hz for MoS_2 NC-FETs with 2 nm Al_2O_3 and 15/20/35 nm HZO as gate dielectric. Normalized I_D noise reduces with thicker HZO suggests the capacitance from HZO layer is negative. Note that the data in Fig. 11-13 are based on at least 3-5 devices measured and averaged.

where N_t is the trap density in the gate dielectric, λ is the tunneling attenuation length (constant in this work), γ is the frequency exponent (≈1 in this work as seen in Fig. 8), C_d is the depletion capacitance and C_{it} is the interface trap capacitance. From eqn. (1), the normalized power spectral density by drain current and area ($W_{ch}L_{ch}*S_{ID}/I_D^2$) vs. I_D is not dependent on oxide thickness in the on-state, hence, our major discussion in this work focuses on the subthreshold regime. In this regime, C_d is the same at a given I_D with the same doping concentration. Therefore, the larger the gate capacitance (C_{ox}) is, the smaller the $W_{ch}L_{ch}*S_{ID}/I_D^2$ would be at the same number of traps N_t and C_{it} in eqn. (2). For conventional MOSFETs, $W_{ch}L_{ch}*S_{ID}/I_D^2$ increases with thicker gate oxide since C_{ox} is decreased as described in eqn. (2). Furthermore, Fig. 11 shows $W_{ch}L_{ch}*S_{ID}/I_D^2$ vs. I_D at 10 Hz frequency for MoS_2 NC-FETs with different 1 nm interfacial oxide layers on 20 nm HZO as the gate dielectric. $W_{ch}L_{ch}*S_{ID}/I_D^2$ is different with different interfacial oxide, showing the oxide traps related to Al_2O_3 interfacial layer are the lowest. Fig. 12 shows $W_{ch}L_{ch}*S_{ID}/I_D^2$ vs. I_D at 10 Hz for MoS_2 NC-FETs but with three Al_2O_3 thicknesses, namely, 0.5 nm, 1nm, and 2 nm and 20 nm HZO as the gate dielectric. Referring to eqn. (2), $W_{ch}L_{ch}*S_{ID}/I_D^2$ should be smaller for thinner Al_2O_3 since the total gate capacitance is larger. The data matches the theoretical prediction from this equation well. We ascribe the part of the larger noise at high current level in the 0.5 nm Al_2O_3 sample to the significant amount of oxide traps inside HZO, which may affect the channel noise directly with only 0.5 nm of Al_2O_3 in between. Therefore, a suitable oxide layer design between HZO and the channel is required for high performance MoS_2 NC-FETs with low noise.

To investigate the effect of the thickness of the ferroelectric HZO, $W_{ch}L_{ch}*S_{ID}/I_D^2$ vs. I_D at f=10 Hz are plotted in Fig. 13 for MoS_2 NC-FETs with 2 nm Al_2O_3 interfacial layer and different HZO thicknesses as gate dielectrics. The HZO thicknesses are 15 nm, 20 nm, and 35 nm. From this figure, the normalized power spectral density $W_{ch}L_{ch}*S_{ID}/I_D^2$ is lower with thicker ferroelectric HZO in the subthreshold regime in significant contrast to the conventional high-k MOSFETs [18, 19]. Based on eqn. (2), this suggests that a larger gate capacitance occurs for a thicker HZO instead. This key result verifies that the NC effect not only provides steep subthreshold slope and enhances on-state and off-state performances, but also can suppress 1/*f* noise in devices. Since the devices in Fig. 13 have the same 2 nm Al_2O_3 as interfacial oxide layer, therefore, the capacitance of the HZO layer must be negative to achieve a larger total gate capacitance for thicker oxide gate stacks. Hence, the exitance of negative capacitance in the ferroelectric HZO can be used to physically explain the noise measurement results.

IV. CONCLUSION

We report on low frequency noise studies on MoS2 NC-FETs for the first time. Devices with various interfacial oxides, different thicknesses of interfacial oxide, and ferroelectric $H_{0.5}Z_{0.5}O$ (HZO) are systematically studied. The low frequency noise is found to decrease with thicker ferroelectric HZO in the subthreshold regime of the MoS_2 NC-FETs, in contrast to the conventional high-k transistors, and interpreted as electrostatic improvement induced by the negative capacitance effect. It concludes that negative capacitance can not only improve the device performance in the on- and off-states, but also suppress the noise of the devices.

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